

COURSE PROSPECTUS

Name of the Group: *VLSI Design Group*

Name of the Course: *Chip Design Associate (O-Level Chip Design)*

Course Code: *QG-04-EH-02593-2024-V1-NIELIT/ (VLN301)*

NSQF Level: *Level 4.0*

Starting Date: *03rd November 2025*

Duration: *450 hours/ 3.0 Months*

Mode: *Offline (NIELIT Calicut Campus)*

Course Coordinator: *Sreejeesh SG- 9447769756 |sreejeesh@nielit.gov.in*

Nanditha NV -nanditha@calicut.nielit.in

Preamble: The “Chip Design Associate” course is crafted to provide students with a strong foundation in VLSI Design and Digital System Development, preparing them for careers in semiconductor and embedded system domains. Beginning with fundamental concepts in electronics and digital design, the course guides learners through the principles of logic design and hardware description languages, with a strong emphasis on Verilog. Students will gain hands-on experience in using industry-standard tools such as Xilinx Vivado for simulation and implementation of digital systems on FPGAs. The curriculum includes structured lab sessions to help students develop, simulate, and synthesize digital modules, progressing from basic combinational circuits to complex state machines and SoC design. In addition, learners will be introduced to ASIC design flow and the nuances of RTL coding for ASIC prototyping. By the end of the course, participants will be equipped with both theoretical insights and practical skills needed to contribute to modern chip design workflows, making them job-ready for roles in FPGA development, ASIC verification, and embedded hardware design

Objective of the Course: The objective of the “Chip Design Associate” course is to equip students with practical skills and foundational knowledge in digital electronics and chip-level hardware design. The course begins with an introduction to basic electronics and CMOS fundamentals, enabling students to identify and understand core digital components. Learners will gain proficiency in operating digital instruments and simulation tools, and in assembling and testing digital circuits. A significant portion of the course focuses on Verilog HDL, where students will learn to model and simulate digital logic using industry-standard design practices. They will work on logic synthesis, timing analysis, and design verification, culminating in FPGA implementation using tools like Xilinx Vivado. Through structured lab exercises and a final project, students will conceptualize, design, and implement digital systems, ranging from basic logic blocks to finite state machines and SoC prototypes. By the end of the course, students will be capable of contributing to VLSI design workflows and FPGA-based hardware development, preparing them for entry-level roles in the semiconductor industry.

Outcome of the Course: By the end of the “Chip Design Associate” course, students will possess advanced proficiency in digital electronics and chip-level design methodologies. They will be adept at analyzing and designing digital circuits, understanding CMOS logic fundamentals, and applying this knowledge to real-world design challenges. Students will demonstrate expertise in Verilog HDL for modeling, simulating, and verifying combinational and sequential logic systems, and will be capable of developing synthesizable RTL code for FPGA-based implementation. They will be skilled in using industry-standard tools like Xilinx Vivado for design simulation, synthesis, and hardware deployment. Through hands-on lab sessions and project work, learners will design and implement digital systems such as ALUs, finite state machines, and custom logic blocks on FPGA platforms. They will also gain exposure to the ASIC design flow and basic verification techniques. Upon completion, students will be fully prepared for entry-level roles in VLSI and semiconductor industries as FPGA developers, front-end design engineers, or digital hardware developers.

Expected Job Roles: Front-End VLSI Design Engineer, RTL Design Engineer

Course Structure:

Sl. No	Module Title	Duration (Hours)			Credit
		Theory	Lab	Total	
1	NOS1: VLSI Fundamentals	25	35	60	2
2	NOS2: Verilog RTL coding for Synthesis	25	35	60	2
3	NOS3: Static Timing Analysis of VLSI Circuits	25	35	60	2
4	NOS4: FPGA Architecture and Programming	25	35	60	2
5	Sub total (A)	100	140	240	08
6	Employability Skills (B)	60			2
7	NOS6:OJT/Project* (C)	150			5
Total Duration/Credit		450			15

Other Contents

I. Course Fees:

General Candidates: Course fee is ₹. 25,000/- (Including NSQF Registration and Exam Fees as applicable)

SC/ST Candidates: Tuition Fees are waived for SC/ST students admitted under SCSP/TSP. However they are required to remit an amount of ₹. 2000/- towards NSQF registration and examination fee at the time of joining. *This amount will be considered as security deposit and will be refunded after*

successful completion of the course on first attempt. If the student fails to complete the course successfully, this amount will be forfeited.

It is mandatory that students attending NSQF aligned courses have to appear for NIELIT NSQF examination conducted by NIELIT Headquarter, New Delhi on fee payable basis. Successful candidates will be issued certificates by NIELIT HQ. If the student fails to clear the exam, **participation** certificates will be issued by NIELIT Calicut on passing the exam conducted by NIELIT Calicut.

Module wise Course Fee: Not Applicable for this course

II. Registration Fee: An amount of ₹.1000/- (nonrefundable) should be paid at the time of registering for the course.

This fee shall be considered as part of course fee, if the student joins the course. If the student does not join for the registered course / any of the registered courses, fee paid shall be forfeited.

SC/ST Candidates: Registration fee is Rs.500/- (nonrefundable)

This fee shall be considered as part of NSQF Registration and exam fees, if the student joins the course. If the student does not join for the registered course / any of the registered courses, fee paid shall be forfeited.

However above the registration fee shall be refunded on few special cases as given below

- Course postponed and new date is not convenient for the student
- Course canceled in advance, well before the admission date

III. Course Fee Structure:

Fees	*Amount for General Candidates	Amount for SC/ST Candidates. (considered as caution/security deposit)	Due Date (on or before)
Registration Fee	₹.1000/-	₹.500/-	During Registration
Advance Deposit	₹. 5,000/-	Nil	30-10-2025
Course Fee	₹. 25,000/-	Nil	03-11-2025 (counseling day)
NSQF Registration & Exams Fee	<i>Included in the Course fee</i>	₹. 2000/- (Refundable on successful completion of course on first attempt)	
Total Fee	₹ 25,000/-	Nil	

**** Advance fee -** After publication of the first selection list, the students in the first selection list have to pay the Advance Deposit within the due date to take the provisional admission. Students in the additional selection list should pay both the Advance and course fees together on or before counseling day. The registration fee will be

added to the caution deposit/course fee if the candidate takes provisional admission.

IV. Eligibility: Any one of the following

- Completed 2nd Year of 3 Years Diploma in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches after class 10th with 1.5 years experience.
- Acquired NSQF Level 3.5 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches.
- Acquired NSQF Level 3 in Electronics and Communication Engineering/ Electrical Engineering/CS/IT and allied branches with 3 years' experience.
- Completed 12th or equivalent in Science with Physics and Maths.

V. Number of Seats: **20**

VI. Selection of candidates: Based on marks in the qualifying exam.

VII. Test/Interview (if applicable): *Not Applicable*

VIII. Counseling/Admission: **03-11-2025**

IX. Important Dates (if applicable):

Last date for applying: **28-10-2025**

Selection intimation through mail/website: **29-10-2025 (after 2 PM)**

Certificate Verification/Admission (online mode): **31-10-2025**

X. Course Timings:

Live sessions covering Theory will be scheduled between 9.30 am to 5.00 pm. Assignments and projects can be done at any time of your convenience and submitted before the deadlines provided. Support for completing lab work/assignments will be provided at scheduled times.

XI. Placement: Placement assistance will be provided.

XII. Lab Facilities

Skilled Manpower Advanced Research and Training (SMART) facility or Virtual Prototyping Lab is set up at NIELIT Calicut as part of Chip to Start-up (C2S) programme of MeitY for the proliferation of advanced VLSI and Embedded system design training, research, and electronics systems development across the country.

Note:-Students are requested to bring Laptop

XIII. Course Contents: [Detailed Course Syllabus /Contents Link](#)

[Click here for General Terms and Conditions – Applicable to all courses](#)