ONLINE INTERNSHIP TRAINING PROGRAM
On
VLSI Design
Covering Analog and Digital Design Flow

Date: 29-June 2026

Course Description:

This is an online program which provides a thorough knowledge about the VLSI Design covering Analog and Digital Design Flows. Two Weeks online training and two week extended lab support for the candidates, total duration of the program is 4 Weeks. Well Experienced Faculties from National Institute of Technology – (NIT Calicut) and National Institute of Electronics and Information Technology- (NIELIT Calicut) will be handling the sessions for all the 10 Days.

Program Objectives

To learn, Practice- Analog and Digital industry standard VLSI Design methodologies. To get exposure in industry standard VLSI Design Tools and Flow.

Who can attend?

Students of Engineering (UG & PG) & MSc (Electronics), PhD scholars, faculty members and professionals from Industry.

Duration

- Proposed length of the training: 10 Days. 20 Hours lecture 30 Hours practicals.
- 2 week Lab support for Practical sessions.

₹ 5, 000/- For Students

₹ 8,000/- For Faculty

₹10,000/- For Industry/Corporate

Delivery Mode: Online. Live classes followed by online assignments over LMS. Students should have Laptop/PC with high speed internet connectivity.

Schedule

Duration	:	2 weeks + 2 week extended practice sessions.	
Starting Date	:	29-June-2026	
		Theory	LAB
Day 1		MOSFET/small signal model/digital switch model/frequency of operation/region of operation (saturation)/CMOS technology – **1 hour** Current mirror, biasing, cascode current mirror- **1 hour**	MOSFET characteristics and current mirror
Day 2		CMOS inverters, static CMOS combinational circuits/any other digital circuit, dynamic circuits – **2 hours**	Inverter – schematic and layout
Day 3		Single stage amplifiers (CS, CD, cascode, folded cascode)/single stage op amp including folded cascode buffer- **2 hours**	CS amplifier
Day 4		Two stage op amp design and compensation – 2 hours	Two stage-op amp
Day 5		Two stage op amp design and compensation – **1 hour** Noise, mismatch, offset, linearity etc and layout in analog circuit design-**1 hour**	Two stage-op amp
Day 6		**Digital Logic Design using Verilog HDL I** Contents : Intro to Digital VLSI Design Flow Intro to Verilog HDL	Simulation Lab Modelsim SE®/ Vivado Design Suite
Day 7		Digital Logic Design using Verilog HDL II	Simulation Lab Modelsim SE®/ Vivado Design Suite
Day 8		Digital Logic Synthesis using EDA Tools-I (Basic of synthesis, introduction to fab files etc.)	Demo for Synthesis Lab- Cadence /Synopsys /open source standards
Day 9		Digital Logic Synthesis using EDA Tools –II (Design considerations for Synthesis, SDC Writing, Synthesis Effort, Timing consideration etc.)	Synthesis Lab- Cadence/ Synopsys/open source standards
Day 10		RTL to GDSII Flow	Demo of flow in industry standard Tool Chain

Certificate: e-Certificate will be mailed to the registered email address after completion of the course.

Course Materials

Lectures Notes will be given to each participant via Learning Management System (LMS)

Coordinators

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