

Fundamentals of Zynq SoC based System Design

(10 Hours Online Course)

Course Overview

The primary objective of this workshop is to equip participants with the essential knowledge and practical skills required to design and implement complex embedded systems using the **Xilinx Zynq-7000** System-on-Chip (SoC) platform. This course bridges the gap between software programming and hardware design, focusing on the powerful synergy between the ARM-based Processing System (PS) and the flexible Programmable Logic (PL). Through a hands-on, lab-intensive approach, students will learn the complete design flow, from initial hardware configuration in Vivado to software application development and debugging in Vitis, culminating in the ability to build sophisticated hardware-accelerated systems

Course Contents

1. Introduction to SoC and Zynq FPGA Architecture
2. Vivado IP Integrator and Zynq Hardware–Software Design Flow
3. AXI Communication and GPIO Interfacing Using Zynq
4. Custom IP Development and PS–PL Communication
5. AXI BRAM and DMA-Based Data Transfer Systems

Learning Outcomes

Upon successful completion of this workshop, students will be able to:

- Clearly articulate the differences between an FPGA, a Microprocessor, and a System-on-Chip (SoC).
- Describe the Zynq-7000 architecture, specifically the relationship between the Processing System (PS) and Programmable Logic (PL).
- Utilize the Vivado Design Suite to create, configure, and synthesize a ZYNQ-based hardware platform.
- Employ the Vitis Unified IDE to develop, debug, and run C/C++ applications on the Zynq's ARM processor.
- Implement robust communication between the PS and PL using AXI peripherals like GPIO, BRAM, and custom RTL IPs.
- Implement high-speed data transfers using the AXI DMA (Direct Memory Access) engine.

Target Audience

- B.Tech Students (ECE,EEE,CSE) /Ongoing & Passed Out
- M.Tech Students
- Faculty and Industry Professionals

Course Details

Mode: Online (LMS Based) – [Self paced, Pre-recorded Videos can be watched 24x7]

Duration: 10 Hours

Lab: Remote Hardware Lab - <https://youtu.be/ZniqlITmOkM>

Fee: ₹1000

Certification: NIELIT Calicut.

Detailed Syllabus.

Day 1: Introduction to SoC and Zynq FPGA Architecture

Introduction to SoC concepts, Zynq architecture, remote lab access, and development tools including Vivado and Vitis.

Day 2: Vivado IP Integrator and Zynq Hardware–Software Design Flow

Introduction to Vivado IP Integrator, Vitis IDE, Zynq block design, and hardware-software application development flow.

Day 3: AXI Communication and GPIO Interfacing Using Zynq

Understanding AXI communication, AXI GPIO peripherals, and implementing switch interfacing applications using programmable logic.

Day 4: Custom IP Development and PS–PL Communication

Development of custom IPs and practical examples demonstrating communication between Processing System and Programmable Logic.

Day 5: AXI BRAM and DMA-Based Data Transfer Systems

Introduction to AXI BRAM, memory interfacing, AXI DMA concepts, and high-speed data transfer implementations.

Course Coordinator

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